A 230-Watt S-Band SiGe Heterojunction Bipolar Transistor

Paul A. Potyraj, *Member, IEEE*, Kenneth J. Petrosky, *Member, IEEE*,
Karl D. Hobart, *Member, IEEE*, Francis J. Kub, *Member, IEEE*, and Phillip E. Thompson, *Member, IEEE*

***Abstract*—Large-area Si/$Si_{1-x}Ge_x$ heterojunction bipolar transistors (HBT's) have been demonstrated with record output power at S-Band. Under pulsed conditions in class C operation, a saturated power in excess of 230 W was achieved at 2.8 GHz. At 200 W the devices exhibited a collector efficiency of 46% and a power gain of 6.9 dB. Devices with implanted Si bases had comparable gain, but only 35% efficiency at 150 W, and saturated at 180 W. In class A operation, 13.5 dB gain was demonstrated at 3.1 GHz on smaller devices. For high f_{max}, a self-aligned silicided polysilicon-emitter structure was used in conjunction with a graded $Si_{1-x}Ge_x$ base. Variable temperature dc tests and accelerated life tests have indicated no reliability problems. The results indicate for the first time that Si/SiGe HBT's are suitable for high-power, high-frequency applications.**

I. Introduction

SYSTEM applications have been driving the development of microwave power devices. Bipolar junction transistors (BJT's) in particular have been investigated because they have a high current-handling capability per-unit-area along with high-voltage operation. Silicon BJT's have been demonstrated with power levels of several hundred watts in pulsed applications at L-Band frequencies (1–2 GHz). However, the RF power, efficiency, and gain of these devices deteriorate as the frequency of operation increases. GaAs heterojunction bipolar transistors (HBT's) have shown good efficiency and power gain through X-Band (8–12 GHz) and beyond, but their power levels have historically been limited to tens of watts or less [1]. Moreover, their cost has made widespread usage less attractive. Cost and level-of-integration usually relegate GaAs devices to that part of the spectrum where Si devices falter. For small-signal applications, this boundary is being pushed toward higher frequency by the introduction of bandgap engineering to the silicon technology base. In particular, silicon HBT's with a $Si_{1-x}Ge_x$ base have been demonstrated which have an f_{max} in excess of 160 GHz [2]. The extension of this technology to microwave power devices has received only limited attention [3], [4].

The objective of this work is to extend the power and frequency range of operation of silicon bipolar transistors to S-Band (2–4 GHz) and beyond through the application of $Si_{1-x}Ge_x$ epitaxial base technology. Incorporation of germanium in the base allows heavier base doping without degradation of the current gain. This results in a lower base sheet resistance and therefore a higher f_{max}. Grading of the Ge concentration in the base and a reduction in the basewidth both serve to decrease the base transit time and hence increase f_T. In general the significance of this reduction may be limited if the cutoff frequency is dominated by the collector transit delay time. To achieve high-power gain, a high collector-base (CB) breakdown voltage is desired, necessitating the use of a relatively thick and lightly doped collector. While such a collector can only degrade f_T, f_{max} could improve due to the reduction in the CB capacitance, and such an approach has led to the SiGe HBT's with the highest reported f_{max} [2].

No added reliability risk is anticipated with the introduction of SiGe, even given the high temperatures associated with power transistors. Rather, narrow bandgap HBT's offer a potential solution to the thermal runaway problem encountered with conventional BJT's, inasmuch as the bandgap offset introduces a term into the current gain that declines as the temperature increases.

II. Base Profile Design

The Ge profile in the base was designed to take advantage of both: 1) higher injection efficiency due to the strain-induced and alloy-bandgap narrowing of $Si_{1-x}Ge_x$ and 2) reduced base transit time t_b due to the drift-field created by bandgap grading. The first can be achieved by using a fixed Ge concentration ("box" profile) while the latter is obtained by employing a ramped profile. To optimize for both properties, a trapezoidal profile was chosen.

The 60-nm wide Ge profile was designed to allow for undoped spacer layers on either side of the 35-nm boron profile and accommodate diffusion during growth and subsequent processing. Given the intended thermal budget, it was empirically determined from test runs and TEM studies that the Ge fraction $x = 0.10$ would be stable throughout the processing sequence (although not expected to be unconditionally stable as per Matthews–Blakeslee [5]). Following the formalism of Harame *et al.* [6], the figure of merit chosen for optimization was the ratio of the current gain enhancement (β_{SiGe}/β_{Si}) to the base transit time reduction ($t_{b,SiGe}/t_{b,Si}$). This parameter is plotted in Fig. 1 as a function of the fraction of Ge that is graded (see inset). Accordingly, the Ge fraction was graded from $x = 5\%$ at the emitter-base (EB) junction to 15% at the CB junction. The base doping of 5E18 cm^{-3} was then determined by targeting a current gain of 100.

III. EPI Growth and Device Fabrication

The collector was formed by growing lightly doped silicon epi via APCVD on highly doped $n(100)$ Si substrates. The

Manuscript received April 1, 1996.

P. A. Potyraj and K. J. Petrosky are with Northrop Grumman ESSD, Baltimore, MD 21203 USA.

K. D. Hobart, F. J. Kub, and P. E. Thompson are with the Naval Research Laboratory, ESTD, Washington, DC 20375 USA.

Publisher Item Identifier S 0018-9480(96)08551-1.

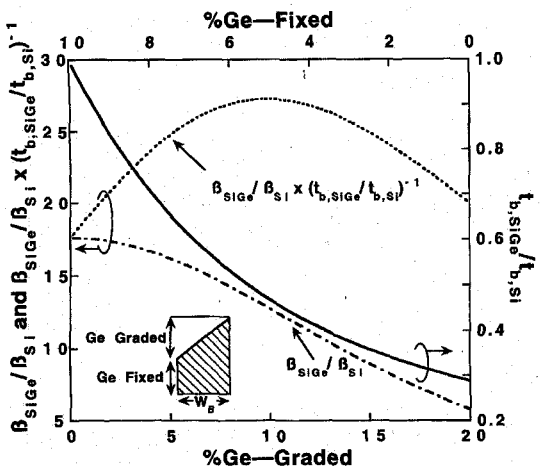


Fig. 1. Base profile optimization curve. The ratio of the current gain enhancement to the base transit time reduction is maximized when Ge-graded is 10% and defined as the difference between the maximum and minimum Ge concentrations.

n^- epi doping profile was chosen subject to three criteria: 1) minimize the CB depletion layer x_d; 2) support the targeted breakdown BV_{CBO}; and 3) provide collector current ballasting to improve ruggedness during a load mismatch. After patterning a field oxide, a p^- moat ring was defined to prevent early breakdown at the perimeter of the base; this facilitates a reduction in x_d for a given BV_{CBO}. After patterning a second field oxide, the wafers were prepared for growth of the base and emitter epi layers.

Following an RCA-type clean, the wafers were dipped in a diluted HF solution and spun dry immediately prior to loading in the MBE system. The in situ boron-doped p^+ SiGe base and undoped Si emitter layers were grown by solid-source molecular-beam epitaxy. Low interfacial boron ($\sim$1E9 cm^{-2}) was achieved through a low-temperature in situ cleaning process that eliminates wafer slip [7].

After removing the SiGe from the field regions, a third oxide layer was defined to minimize the active emitter-base area. For the emitter contact, polysilicon was deposited in a conventional LPCVD reactor, implanted with phosphorus, and capped with nitride. Prior to poly deposition, the wafers were precleaned using an RCA-type clean followed by an HF vapor clean with no rinse. Using conventional lithography, 0.8-μm emitter stacks were then defined by reactive-ion etching. Subsequently, an oxide spacer was formed at the perimeter of the emitter to isolate it from the extrinsic base region. To ensure contact to the intrinsic base, boron was implanted before and after the sidewall spacer was formed. After removing the nitride from the emitter stack, the wafers were annealed for 15 minutes at 750°C. A schematic cross section and SIMS profile are shown in Figs. 2 and 3. Platinum was used to form a self-aligned silicide over the entire emitter-poly and extrinsic base regions, ensuring low parasitic-base resistance. The devices were contacted using a double-level Au lift-off metallization scheme which includes TiW resistors for emitter ballasting.

HBT's fabricated as described above were compared to existing silicon BJT's made using the same mask set. The latter was produced using the same basic process but with several differences: 1) no Ge was present in the base; 2) the base was ion-implanted instead of epitaxially grown; 3) the emitter anneal was at 950°C; and 4) n(111) substrates were used. The last factor is not considered significant.

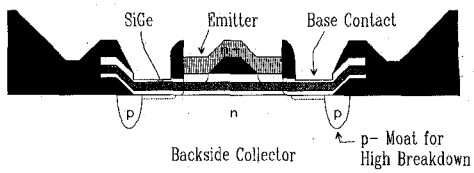


Fig. 2. Schematic cross section of a single element of the SiGe HBT fabricated.

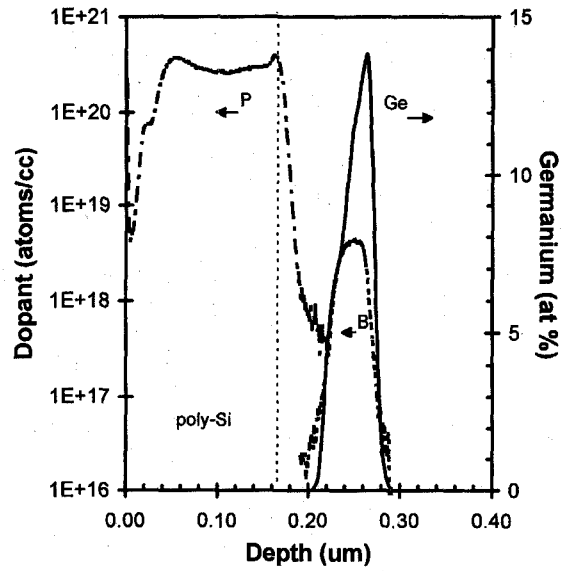


Fig. 3. SIMS data showing the vertical profile through the polysilicon, emitter, and base for the HBT.

IV. DC Characterization

Devices were characterized for dc and high-power RF performance. DC measurements are summarized in Table I, and Gummel plots are shown in Fig. 4. Although the table indicates higher breakdown voltages for the Si parts, it is believed that this is partially attributable to unintentional variations in the collector profile. To support the high voltages necessary for a power transistor, both parts were designed for a breakdown of $BV_{\mathrm{CBO}} = 60$ V with $N_C = 3\mathrm{E}15$ cm^{-3} at the CB junction; however four-point probe data indicates nearly 25% higher resistivity for the collector of the Si BJT. Device geometry may also affect the breakdown; the field termination employed was developed for an implanted base device and may not be optimized for a planar epitaxial base device. Measurements on other high-voltage devices showed no degradation in breakdown when a SiGe base was used [3].

The improvement in the current gain and Early voltage product βV_A from the Ge doping is tempered by differences in the emitter anneal for the two types of parts. Moreover, the devices characterized in Table I were designed to achieve high-current density at microwave frequencies and therefore

TABLE I
COMPARISON OF THE DC PARAMETERS FOR THE SiGe HBT AND Si BJT; $P_E = 4240\ \mu$m, $A_E = 1320\ \mu$m^2, and $A_B = 7000\ \mu$m^2

Type		SiGe	Si
Lot		LE8177-4	LE8352-4
BV_{CBO}	V	62	76
BV_{CEO}	V	39	55
BV_{CES}	V	62	75
β_{max}	-	95	120
V_A	V	110	80
$\beta_{max}V_A$	V	10450	9600
n_B	-	1.17	1.20

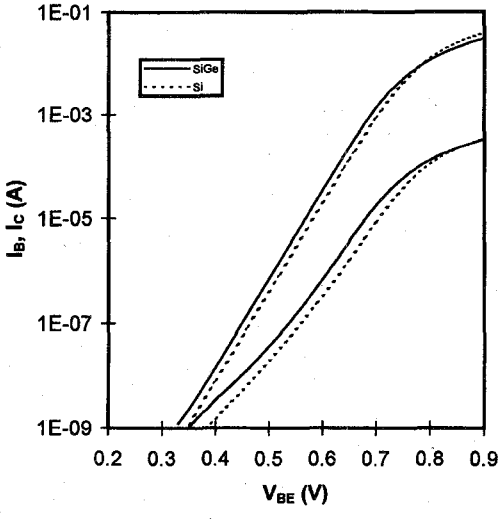


Fig. 4. Gummel plots measured at $V_{CE} = 3$ V; $P_E = 4240\ \mu$m, $A_E = 1320\ \mu$m^2, and $A_B = 7000\ \mu$m^2.

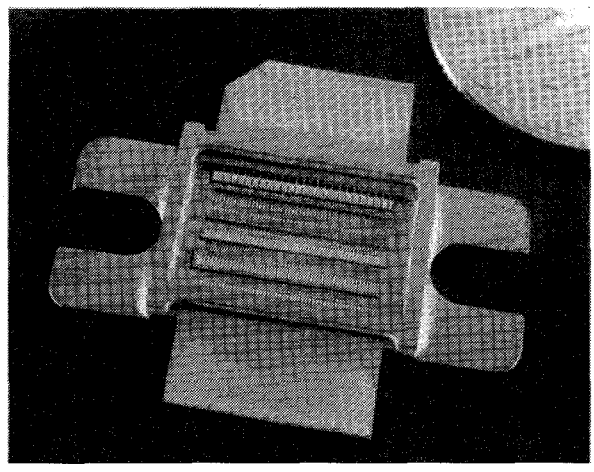


Fig. 5. Photograph of a 230-W packaged device including internal matching network.

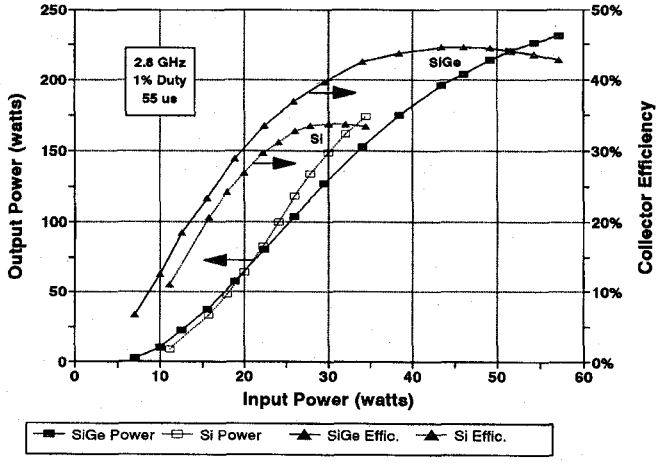


Fig. 6. Output power and collector efficiency at 2.8 GHz for a 55-μs pulsewidth in class C operation with 40-V bias; $P_E = 590$ mm, $A_E = 0.26$ mm^2, and $A_B = 0.91$ mm^2.

employ a very high ratio of emitter periphery to the base area. When large dc test transistors were probed, βV_A was 31 kV.

The emitter anneal difference would also likely result in higher emitter resistance for the SiGe device, which might then account for its sharper high-current rolloff as seen in the Gummel plot of Fig. 4. A similar effect is seen during regression measurements (measured I_C versus forced V_{BE} for a fixed collector voltage, as in the Gummel plot, but with forced I_B). However, it is difficult to unambiguously attribute these effects to emitter resistance if we assume: 1) self-heating is an issue at high currents and 2) the HBT's current gain is less sensitive to temperature so that the device is less susceptible to thermal runaway. As will be seen, the data confirms the latter assumption.

V. RF CHARACTERIZATION

Small-signal ac (s-parameter) measurements were performed on-wafer for the devices of Table I to extract the cutoff frequency f_T. Testing under the targeted operating bias of 40 V led to severe thermal dissipation problems, and the bias had to be reduced to 10 V. At 50 mA, the extracted f_T for both the Si and SiGe devices peaked at 4.2–4.4 GHz. These values were calculated without fully deembedding the parasitics contributed from the silicon substrate. In particular, the calibration technique did not account for the pad-to-substrate capacitance, a term which typically affects measurements on silicon substrates much more than on GaAs. Moreover, the values are believed to be depressed by the use of a relatively resistive top-side collector contact.

For high-power RF testing, large area devices with the same periphery to area ratio as in Table I were used. A single chip containing multiple transistor cells is packaged in a common-base configuration with an internal matching network targeted for operation from 2.7–2.9 GHz. Precise wire bonding is performed in an automated system with pattern recognition and stitch-bond capability (Fig. 5). The total emitter periphery is $P_E = 590$ mm, with a base area $A_B = 0.91$ mm^2, believed to be the largest HBT reported to date. The devices were tested in class C operation under pulsed conditions with a pulsewidth of 55 μs and a duty cycle of 1–7%. The dc bias on the output (collector) was 40 V, and the RF input power varied from 0 to 60 watts. The RF output power and collector efficiency at 2.8 GHz are shown in Fig. 6. The Si parts failed catastrophically at power levels near 180 W. The SiGe parts exhibited similar RF gain but continued to operate well past 200 W. The testing

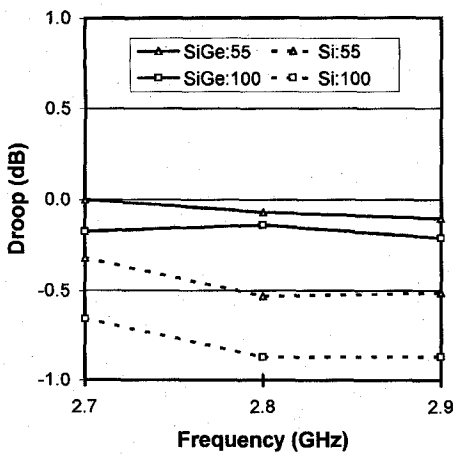


Fig. 7. Droop in the pulse envelope for pulsewidths of 55 and 100 μs. SiGe devices at 180 W are compared to commercial Si parts at 140 W. Despite running at higher power, the SiGe devices show substantially less droop.

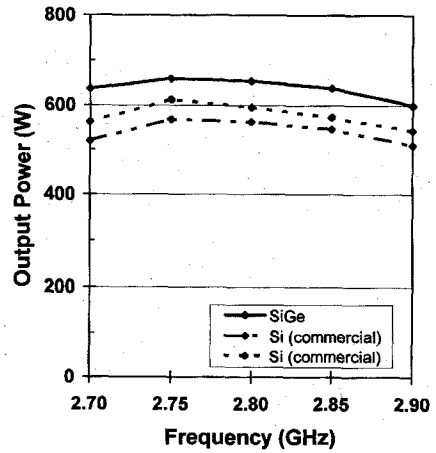


Fig. 8. Output of a power amplifier module with four devices in the output stage. SiGe devices are compared to typical commercial Si parts.

was discontinued at 235 W, at which point the incremental power gain was declining rapidly. While the SiGe part tested here reached 46% efficiency, the Si part never exceeded 35%. For an output of 180 W, the Si part must then dissipate 110 watts more than the SiGe part. Subsequent testing on similar SiGe transistors gave peak efficiencies above 50%. At 180 watts, the efficiency and power gain were 48% and 6.9 dB. On smaller devices for which combining losses are not as great, the efficiency was 55% at comparable power densities.

The SiGe transistors also proved to be rugged, passing a 3:1 VSWR stress test as well as a 2-dB overdrive test applied during 180-W output power. Pulse droop was negligible under matched conditions and was only 0.2 dB during a 3:1 VSWR. As the pulsewidth was increased to 100 μs, droop remained below 0.2 dB across the band, demonstrating a marked improvement over commercially available Si parts (Fig. 7). This data suggests that concerns over the ability of an HBT to run at the elevated temperatures typical of a power device are unfounded.

Several HBT's were packaged and tested with consistent results. Five of these devices were assembled into a power module using a one-driving-four architecture. The combined output power was 600–660 W across the band for 2.7–2.9

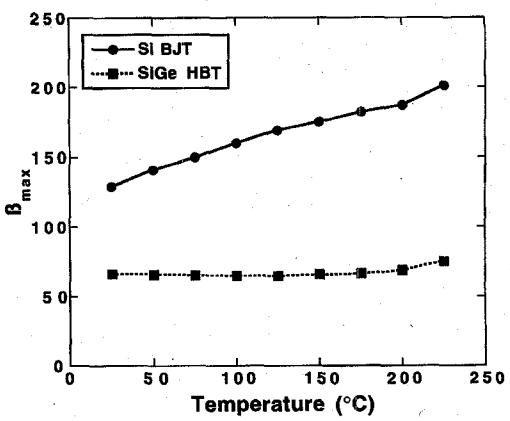


Fig. 9. Maximum current gain as a function of case temperature for the HBT's and BJT's fabricated here.

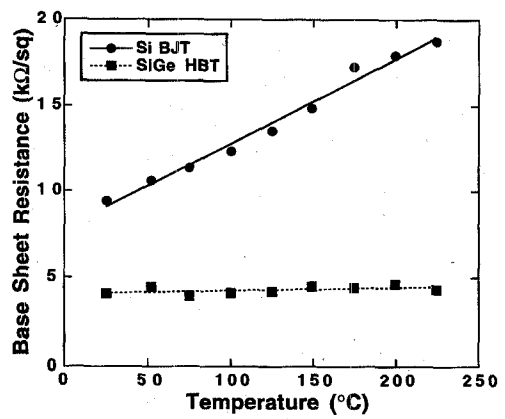


Fig. 10. Base pinch resistance as a function of case temperature.

GHz, an improvement of 10–15% over that typically obtained using commercially available Si devices (Fig. 8).

A limited amount of testing was also performed with devices biased in class A mode where substantially higher gain was observed. For moderate-sized devices (P_E = 296 mm and A_B = 0.45 mm^2) tested under a pulsewidth of 25 μs and duty cycle of 1%, 12.2-dB gain was demonstrated at 50-W output power at 3.1 GHz with a collector voltage of 32 V. At lower power the gain was 13.5 dB at 3.1 GHz and remained above 10 dB at 3.3 GHz.

VI. Reliability and High-Temperature Effects

Given the concerns over the reliability of SiGe HBT's in general and the hostile environment typical for microwave power transistors, high-temperature measurements and burn-in studies were initiated. Variable-temperature dc measurements were made to determine the effect of the heterojunction on the device performance. The heterojunction effect will counter the bandgap narrowing in the heavily doped emitter. Although the HBT's presented here were not optimized for high-temperature operation, the devices nonetheless behaved well at elevated temperatures. Fig. 9 displays $\beta_{\max}$ over a temperature range that exceeds worst-case operating conditions. The current gain of the Si BJT increased as expected, but the SiGe HBT exhibited negligible variation up to 225°C, indicating that the

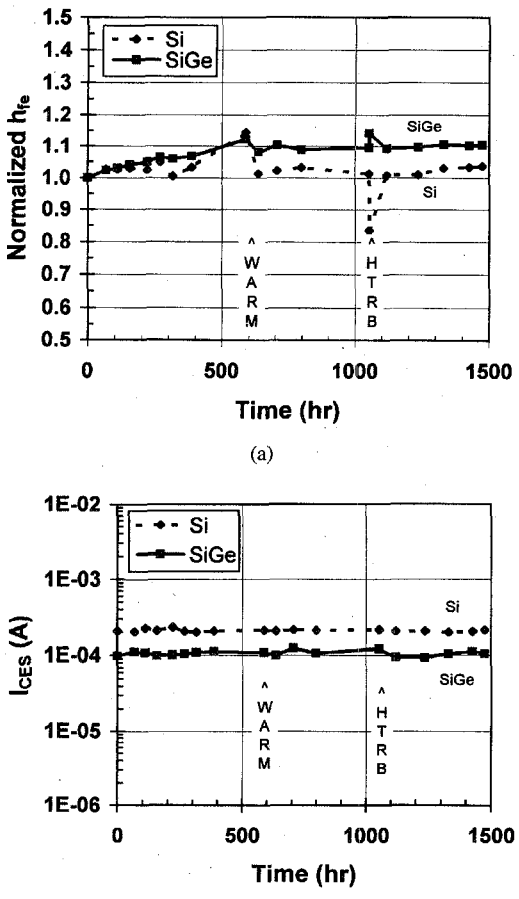


Fig. 11. Effect of accelerated life testing. (a) The normalized current gain and (b) the collector-emitter leakage current. The straggle in the leakage current is attributed to measurement error.

HBT's have an internal mechanism that may reduce thermal runaway and the need for external ballasting. The behavior of the current gain at lower collector currents was comparable. The pinched base resistance also exhibited remarkably similar behavior (Fig. 10). While not fully understood, this result suggests that $f_{\max}$ and hence the power gain are likely to be more stable for the HBT's. This stability, coupled with the lower base resistance, may then contribute to the improved performance of the HBT's at high-power densities. The HBT's also fared better at cryogenic temperatures. At 77 K, $\beta_{\max}$ for Si dropped to 5% of its value at room temperature while for SiGe, it increased by 70%.

To more directly investigate the issue of reliability, a small sample of very large devices ($P_E = 1.09$ m and $A_B = 1.8$ mm^2) were subjected to a forward-bias burn-in ($V_{CE} = 5$ V and $I_E = 0.5$ A) which stresses the junction at 170°C. Fig. 11 displays the effect on: 1) the normalized low-current incremental current gain h_{fe} and 2) the emitter-collector leakage current I_{CES} ($V_{CE} = 40$ V) after nearly 1500 h of stress. Briefly, both the Si and the SiGe devices behaved well with little or no degradation in leakage current and with a slight increase in current gain. After 1000 h, the forward-bias burn-in was interrupted, and a 70-h high-temperature reverse-bias (HTRB) stress test was instituted at a junction temperature of 150°C and bias of $V_{CBO} = 45$ V. This depressed the current gain of the Si components but elevated the gain for the SiGe parts. No detrimental effect on leakage current was seen. All devices returned to their pre-HTRB values when the forward-bias burn-in was resumed. The temporary excursion in current gain at 590 h is attributed to inadvertently testing the devices while still warm from the burn-in and thus, not viewed as significant.

VII. Conclusion

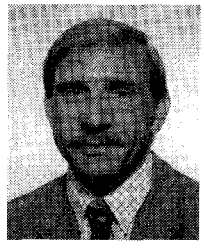
Large-area, high-perimeter epitaxial-base SiGe HBT's were fabricated and compared to implanted-base Si BJT's. It was found that the HBT's were suitable for the application of pulsed high-power transistors at S-Band and yielded significant performance improvements. The characteristics of the HBT's had substantially less dependence on temperature and behaved comparably to the Si BJT's during accelerated life tests.

Acknowledgment

The authors would like to acknowledge the contributions from J. Ostop and P. Esker for assistance with matching, assembly, and the RF test and L. Ardis and the ATL foundry for wafer preparation and fabrication.

References

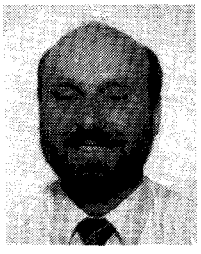
[1] T. Shimura *et al.*, "1 W Ku-band AlGaAs/GaAs power HBT's with 72% peak power-added efficiency," *IEEE Trans. Electron Devices,* vol. 42, no. 11, p. 1890, 1995.
[2] A. Schüppen *et al.*, "Enhanced SiGe heterojunction bipolar transistor process with 160 GHz $f_{\max}$," in *IEEE Int. Electron Devices Meet. Tech. Dig.,* 1995, p. 743.
[3] K. D. Hobart *et al.*, "Si/Si$_{1-x}$Ge$_x$ heterojunction bipolar transistors with high breakdown voltage," *Electron Device Lett.,* vol. 16, no. 5, p. 205, 1995.
[4] P. A. Potyraj *et al.*, "A 230 Watt S-Band SiGe HBT," in *IEEE MTT-S Int. Microwave Symp. Dig.,* vol. 2, 1996, p. 673.
[5] J. W. Matthews *et al.*, *J. Cryst. Growth,* vol. 27, p. 118, 1974.
[6] D. L. Harame *et al.*, "Optimization of SiGe HBT technology for high speed analog and mixed-signal applications," in *IEEE Int. Electron Devices Meet. Technical Dig.,* p. 71, 1993.
[7] P. E. Thompson *et al.*, *J. Vac. Sci. Technol. B, Microelectron Process. Phenom.*, vol. 11, p. 1077, 1993.



Paul A. Potyraj (S'85–M'87) received the B.A. degree in physics from Johns Hopkins University, Baltimore, MD, in 1982 and the M.S. and Ph.D. degrees in physics from Carnegie Mellon University, Pittsburgh, PA, in 1984 and 1987, respectively.

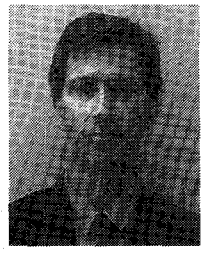
After completing his thesis on polysilicon-emitter transistors, he joined Westinghouse Electronic Systems Division, Baltimore (acquired by Northrop Grumman Corporation in 1996). Since then he has worked as a Device Physicist and Process Development Engineer for the SiGe HBT, Si Microwave-Power Transistor, Si MMIC, and Submicron CMOS programs. Currently an Advisory Engineer with Northrup Grumman, he is the Principal Investigator for SiGe HBT's and the Lead Process Development Engineer for polysilicon-emitter microwave transistors. He has 12 years of experience in the fabrication of advanced silicon devices with a concentration in high-frequency applications. He has authored or co-authored ten research papers and seven patent disclosures on semiconductor technology.

Dr. Potyraj is a Member of the Electrochemical Society.



Kenneth J. Petrosky (S'69–M'71) received the B.S.E.E. and M.S.E.E. degrees at Carnegie Mellon University, Pittsburgh, PA, in 1970 and 1971, respectively.

He has 25 years of experience at Westinghouse/Northrop Grumman, Baltimore, MD, in analog design encompassing a variety of systems and circuitry, from low-frequency applications of control systems and SONAR processors to the high-frequency world of A/Ds, high-speed CCD's, and microwave devices. Currently, he is a Senior Advisory Engineer with Northrop Grumman. His primary responsibility is the technical direction and program management of all silicon bipolar-power transistor programs. His technical contributions have included the die design and layout for the various transistors and the internal matching designs for specific applications. He has written 20 disclosures and holds six patents.

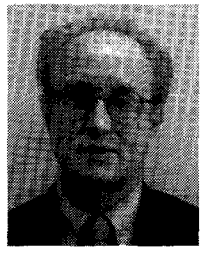


Karl D. Hobart (S'87–M'91) received the B.S. degree in physics from the University of Illinois at Urbana-Champaign in 1984. He received the M.S.E.E. and Ph.D. degrees in electrical engineering from the University of Delaware, Newark, in 1987 and 1991, respectively.

From 1991 to 1993, he worked as a Post Doctoral Research Fellow at the Naval Research Laboratory in Washington, DC. He is currently a permanent Staff Member of the Electronics Science and Technology Division at the Naval Research Laboratory. His research interests include group IV heteroepitaxy, SiGe HBT's, and direct-wafer bonding.

Francis J. Kub (S'75–M'78) was born in Aberdeen, SD, on March 25, 1949. He received the B.S. degree in engineering physics from South Dakota State University, Brookings, in 1972, the M.S.E.E. degree from the University of Minnesota, Minneapolis, in 1974, and the Ph.D. degree in electrical engineering from the University of Maryland, College Park, in 1985.

Since 1985, he has worked at the Naval Research Laboratory in Washington, DC, where he is the Supervisor of the Microelectronic Device Physics Section. His research interests include the areas of analog VLSI for artificial neural networks and adaptive filters, photodetector design for acoustooptic signal processing, and new silicon device development. Prior to joining the Naval Research Laboratory, he worked for the Westinghouse Advanced Technology Laboratory, Baltimore, MD, in the area of submicrometer VHSIC process development and CCD device physics and process technology.



Phillip E. Thompson (S'92–M'96) was born in York, PA, on November 14, 1946. He received the B.S. degree with honors in physics from Lebanon Valley College, Annville, PA, in 1968 and the Ph.D. degree in physics from the University of Delaware, Newark, in 1975.

He was an Assistant Professor of Physics at Lebanon Valley College from 1974 to 1981. Since 1981 he has been a Research Physicist at the Naval Research Laboratory, Washington, DC. At the present time he heads the Si MBE Growth and Characterization Section. His initial work was in ion implantation where he established procedures for the formation of isolating regions in InP using ion implantation. He performed the fundamental studies on the use of high-energy (1–20 MeV) implantation in GaAs beginning with range measurements and activation techniques and ending with demonstration devices. Since 1988, his research emphasis has been on the growth and characterization of epitaxial films grown by molecular-beam epitaxy. From 1988 to 1990, the research focus was on InSb and InAsSb heterostructures for infrared detector applications. Since 1990, the research emphasis has been on the growth of SiGe with a VG-80 MBE system. Fundamental studies have been published on Si surface-preparation techniques to minimize contamination, temperature dependence of Sb doping of Si, the effect of growth temperature on impurity distribution in SiGe multiple-quantum wells (MQW), optical properties of SiGe MQW, and SiGe HBT's. He has authored or co-authored more than 80 journal articles and holds two patents.

Dr. Thompson is a member of the American Physical Society and the Materials Research Society.